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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
**Patent Application**

Inventor(s): Schieck et al. Confirmation No.: 7655

Application No.: 10/789,637 Group Art Unit: 2822

Filed: February 27, 2004 Examiner: K. DUONG

Title: A FLIP CHIP SEMICONDUCTOR DIE INTERNAL SIGNAL ACCESS SYSTEM AND METHOD

**Form 1449**

**U.S. Patent Documents**

Examiner Initial	No.	Publ./Patent No.	Date	Patentee	Class	Sub-class	Filing Date
KBD	A	2001/0010356	8/2/01	Talbot et al.	250	307	2/10/01
	B	2001/0006233	7/5/01	Vallett	257	48	1/29/01
	C	2003/0119297	6/26/03	Am et al.	438	612	1/27/03
	D	5,258,648	11/2/93	Lin	257	778	11/27/92
	E	6,081,429	6/27/00	Barrett	361	767	1/20/99
	F	6,686,615	2/3/04	Cheng et al.	257	208	8/20/02
✓	G	6,307,162	10/2/01	Masters et al.	174	262	12/9/96
	H						
	I						
	J						
	K						

**Foreign Patent or Published Foreign Patent Application**

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation
							Yes No
KBD	L	19515591	10/19/95	DE	H0L	23/525	
	M						
	N						

**Other Documents**

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	R	
	S	
	T	
Examiner	<i>Johnh Duong</i>	Date Considered <i>4/15/2006</i>

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.  
 Include copy of this form with next communication to applicant.